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10/618,163	07/11/2003	Tsutomu Yamada	YKI-0093-C	4359

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,163	YAMADA, TSUTOMU	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6 and 8-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida et al., U.S. Patent No. 6,133,074.

Ishida anticipates a method for manufacturing a semiconductor device comprising the steps of:

in fig. 6C, forming a metal layer 11 over a partial region of a transparent substrate 71;

in fig. 6E, forming a buffer layer 80 covering the metal layer;

forming an amorphous semiconductor film 63 above the buffer layer so that the amorphous semiconductor film at least partially overlaps the formation region of the metal layer with the buffer layer therebetween; and

polycrystallizing the amorphous semiconductor film through laser annealing to form a polycrystalline semiconductor film 83, col. 8, line 12 - col. 9, line 8;

wherein the buffer layer alleviates thermal leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing, due to the nitride layer 78 covered by an oxide layer 79, col. 8, lines 57-63;

limitations from claim 5: in fig. 5, a method for manufacturing a semiconductor device according to claim 1, wherein the polycrystalline semiconductor film 81 forms an active layer 93 of a thin film transistor, col. 7, lines 12 - 41.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claims 1, 2, 5 above.

Ishida does not limit the thickness of the buffer film formed by the nitride layer 78 and the oxide layer 79, but leaves the practitioner to optimize these dimensions.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentablility to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 6, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, U.S. Patent No. 6,573, 955 B2, in view of Ishida.

Murade teaches a method for manufacturing an active matrix display device wherein the active matrix display device comprises a pixel portion and a driver portion, not shown, but described in col. 12, lines 14-20, formed on a same substrate, the pixel portion having a plurality of pixels each comprising a pixel thin film transistor and a display element and the driver portion having a plurality of driver thin film transistors for outputting a signal for driving each pixel in the pixel portion, necessary for creating a display, the method comprising the steps of:

in fig. 3A, selectively forming a metal layer 7 above the substrate 10 such that the metal layer is not formed over the formation region of the driver thin film transistor and is present over the formation region of the pixel thin film transistor, col. 10, lines 32-54;

in fig. 3B, forming, as a buffer layer, a silicon nitride film or a silicon oxide film 11 in over almost the entire surface of the substrate and covering the metal layer, col. 10, lines 55-63;

forming a polycrystalline semiconductor film 1 over the buffer layer above the formation region of the pixel thin film transistor and above the formation region of the driver thin film transistor, col. 10, lines 55-63; and

in fig. 3E, forming a gate electrode 2 above the obtained polycrystalline semiconductor film with a gate insulation film 12 therebetween to obtain a pixel thin film transistor and a driver thin film transistor each having, as an active layer, the polycrystalline semiconductor film obtained respectively in the formation region of the pixel thin film transistor and the formation region of the driver thin film transistor, col. 10, line 63 - col. 12, line 20.

Murade does not specify forming an amorphous film over a two layer buffer layer and then crystallizing with a laser beam, but Ishida does. Ishida teaches a method for manufacturing a semiconductor device comprising the steps of:
in fig. 6C, forming a metal layer 11 over a partial region of a transparent substrate 71;
in fig. 6E, forming a buffer layer 80 covering the metal layer;
forming an amorphous semiconductor film 63 above the buffer layer so that the amorphous semiconductor film at least partially overlaps the formation region of the metal layer with the buffer layer therebetween and simultaneously forming a second amorphous semiconductor film above the non-formation region of the metal layer; and
polycrystallizing the first, above metal layer 11, and second amorphous semiconductor

films, above metal layer 12 through laser annealing to form a first polycrystalline semiconductor film and a second polycrystalline semiconductor film, and forming a polycrystalline semiconductor film 83, col. 8, line 12 - col. 9, line 8; wherein the buffer layer alleviates thermal leakage caused by thermal conduction in the metal layer during polycrystallization of the amorphous semiconductor film through laser annealing, due to the nitride layer 78 covered by an oxide layer 79, col. 8, lines 57-63;

limitations from claim 10: in fig. 5, a method for manufacturing a semiconductor device according to claim 1, wherein the polycrystalline semiconductor film 81 forms an active layer 93 of a thin film transistor, col. 7, lines 12 - 41;

limitations from claim 12: a method for manufacturing an active matrix display device according to claim 11, in fig. 5, wherein each pixel further comprises a storage capacitor SC, which has a first electrode electrically connected to the active layer of the pixel thin film transistor, and a second electrode of the storage capacitor is formed by the metal layer 12, col. 7, lines 53 - col. 8, line 11.

For claims 8-9, Ishida does not limit the thickness of the buffer film formed by the nitride layer 78 and the oxide layer 79, but leaves the practitioner to optimize these dimensions.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentablility to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical

ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claims 1, 5 above, and further in view of Miyanaga et al., U.S. Patent No. 5,705,829.

Ishida does not specify forming grains in the first polycrystalline semiconductor film in appropriate range and different from each other, but Miyanaga does. Miyanaga teaches in figs. 2A-F forming amorphous silicon regions 203 in the peripheral circuit thin film transistors and polycrystallization by laser annealing, and in figs. 3A-F forming amorphous silicon regions 203 in the pixel thin film transistors and polycrystallization by laser annealing, col. 4, line 22 - col. 6, line 31, wherein the first polycrystalline semiconductor film and the second polycrystalline semiconductor film comprise grain

sizes within an appropriate range and different from each other, col. 6 lines 24-31, wherein the main sizes are formed during the laser annealing of the first amorphous semiconductor film and the second amorphous semiconductor film, col. 5, line 62 - col. 6, line 4. Miyanaga gives motivation in col. 1, lines 27-33. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Miyanaga's process with Ishida's invention would have been beneficial because the invention because pixel and peripheral TFTs have different mobility and leak current needs.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade in view of Ishida as applied to claims 6, 8-12 above, and further in view of Miyanaga.

Ishida does not specify forming grains in the first polycrystalline semiconductor film in appropriate range and different from each other, but Miyanaga does. Miyanaga teaches in figs. 2A-F forming amorphous silicon regions 203 in the peripheral circuit thin film transistors and polycrystallization by laser annealing, and in figs. 3A-F forming amorphous silicon regions 203 in the pixel thin film transistors and polycrystallization by laser annealing, col. 4, line 22 - col. 6, line 31, wherein the first polycrystalline semiconductor film and the second polycrystalline semiconductor film comprise grain sizes within an appropriate range and different from each other, col. 6 lines 24-31, wherein the main sizes are formed during the laser annealing of the first amorphous semiconductor film and the second amorphous semiconductor film, col. 5, line 62 - col.

6, line 4. Miyanaga gives motivation in col. 1, lines 27-33. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Miyanaga's process with Mirada's and Ishida's invention would have been beneficial because the invention because pixel and peripheral TFTs have different mobility and leak current needs.

Response to Arguments

Applicant's arguments filed 22 October 2004 have been fully considered but they are not persuasive. Applicants argue in pp. 7-10 that 1) Ishida forms a gate electrode and gate insulator which does not represent a metal layer and a buffer layer of the claim, 2) Ishida's buffer layer does not alleviate leakage caused by thermal conduction, 3) that Ishida forms SOG film, not specified by the application's claims, and 4) Murade fails to recognize the thermal leakage and hence is improperly combined.

Examiner respectfully disagrees. For argument 1) applicant argues that Ishida's structure is "differ from each other not merely in their name, but fundamentally in their functions" from the independent claim features. While examiner stipulates that there are differences between the prior art of record and the disclosed application, the USPTO tasks the examiner to interpret the claims broadly as reasonably possible (see below). Whatever the differences may be, the claims as currently amended do not reasonably distinguish themselves from the process features of Ishida, the metal layer may be the gate electrode, and the buffer layer may be the gate insulating layer. For argument 2) Ishida's buffer layer does function to prevent the thermal conduction

caused by the thermal conduction in the metal layer. This is evidenced that Ishida's forms his buffer layer due to the nitride layer 78 covered by an oxide layer 79, col. 8, lines 57-63 cited in the rejection above. Applicant discloses pp. 6-7, ¶ 34 that the application's buffer layer is made from a multilayer structure of nitride and oxide. With Ishida using the same materials in the same-formed structure of a buffer layer, the effects of thermal leakage alleviation would naturally be the same. For argument 3) the independent claims do not specifically exclude the use of spacers. For argument 4), while neither Ishida nor Murade each disclose the full totality of the limitations for which they were combined in a §103 rejection, this is not unexpected. In a §103 rejection, the combination of the prior art is considered in rejection of the claim(s).

It is established that "the test for obviousness is not [an] express suggestion of the claimed invention in any or all of the references but rather what the references taken collectively would suggest to those of ordinary skill in the art." *In re Rosselet,* 146 USPQ 183, 186 (CCPA 1965). See also *In re Jones*, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988).

Examiner must give claims their broadest reasonable interpretation, MPEP §2111, "During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during prosecution and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified, *In re Pratter*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51

(CCPA 1969), *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)." Also see *In re Zletz*, 13 USPQ 2d. 1320 (Fed. Cir. 1989).

For the above reasons, the rejections are deemed proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

5 November 2004
WB